The Examiner states in part:

> As per claim 1, Dias discloses supplying a
> variable voltage to said memory integrated
> circuit (abstract, figure 5 and column 2,
> lines 11-14) and generating address and
> control signals (column 14, lines 14-22 and
> figure 5).

> As per claim 21, Dias discloses supplying a
> variable voltage to said memory integrated
> circuit (abstract, figure 5 and column 2,
> lines 11-14) and supplying different
> voltages during different periods (figure
> 5, abstract and column 14, lines 14-22).

> As per claim 23 Dias discloses supplying a
> variable voltage to said memory integrated
> circuit (abstract, figure 5 and column 2,
> lines 14-22 and figure 5).

Dias et al does not disclose a variable voltage as the
Examiner asserts, nor does Dias et al disclose different
voltages during different periods as the Examiner asserts.
Rather, Dias et al discloses means for maintaining a regular
supply voltage to a DRAM after a power supply failure has
occurred. Dias et al states "When a power fault is detected,
the controller provides the DRAMS with both a <u>regular supply
voltage</u> and appropriately timed refresh signals" (Abstract,
emphasis added).

Dias et al fails to disclose or suggest the invention
recited in Claim 1 as amended which reads in part "...variable
voltage being less during...periods of no data access activity
than during...periods of data access activity....".

Dias et al also fails to disclose or suggest the invention
recited in Claim 21 which reads in part "means to supply to
said memory integrated circuit a first voltage during said
first operation period, a second voltage different from said
first voltage during said second operation period, and a third
voltage different from said first and second voltages during
said third operation period."

Dias et al fails to disclose or suggest the invention
recited in Claim 23 as amended which reads in part "...said

variable voltage being less during periods of no data access
activity than during periods of data access activity..."

In view of the amendments to claims 1 and 23 and in view
of the above discussion, Applicant respectfully requests that
the rejection of claims 1-23 be withdrawn.

The Examiner rejected claims 1-23 under U.S.C. § 102(e) as
being clearly anticipated by Fung. The rejection is
respectfully traversed.

Fung does not disclose "supplying a variable voltage to..
memory integrated circuit" as the Examiner asserts, nor does
Fung disclose "supplying different voltages at different
periods" to a memory as the Examiner also asserts. Rather,
Fung discloses several _other_ ways of reducing power consumption
in a computer. Fung states "During periods of inactivity,
power consumption is reduced in different ways, for example, by
reducing clock speeds or removing clocks, and/or by _removing
power_, and/or by controlling the refresh frequency to memory."
(Fung column 3, line 66 to column 4, line 2, emphasis added).
The term _removing power_ refers to switching power off when not
needed by means of switches in switch unit 22 (Fig. 1).

Fung fails to disclose or suggest the elements of claims
1, 21 and 23 recited above in the discussion of the rejection
in view of Dias et al. Therefore, Applicant respectfully
requests withdrawal of the rejection based on Fung of claims 1-
23.

Claims 1 and 23 as amended are supported in the
application, for example, where it is stated "Hence, during
periods of no data access activity, a minimal voltage is
supplied to memory. During periods of data access activity, a
greater operational voltage is supplied to memory." (page 6,
lines 6-9).

Claim 8, as amended for clarification, is supported in the
application by the statement "For DRAMs, data access activity

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includes both memory refresh and memory access." (page 6, lines 11-12). and by Fig. 2b in which standby periods are shown and by the discussion of Fig. 2b at page 13, lines 16-20.

Claims 1-23 are believed to be allowable. It is respectfully requested that claims 1-23 be allowed and that the application be passed to issue. If there are any questions, the Examiner should call the undersigned at (408) 453 9200.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C., 20231, on July 26, 1996.

July 26, 1996
Date of Signature

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